以多迴路遲滯架構實現
高效能低壓降壓轉換器之設計與模擬

Design and Simulation of High-Efficiency Low-Dropout Buck Converter with Multi-Loop Hysteresis Architecture

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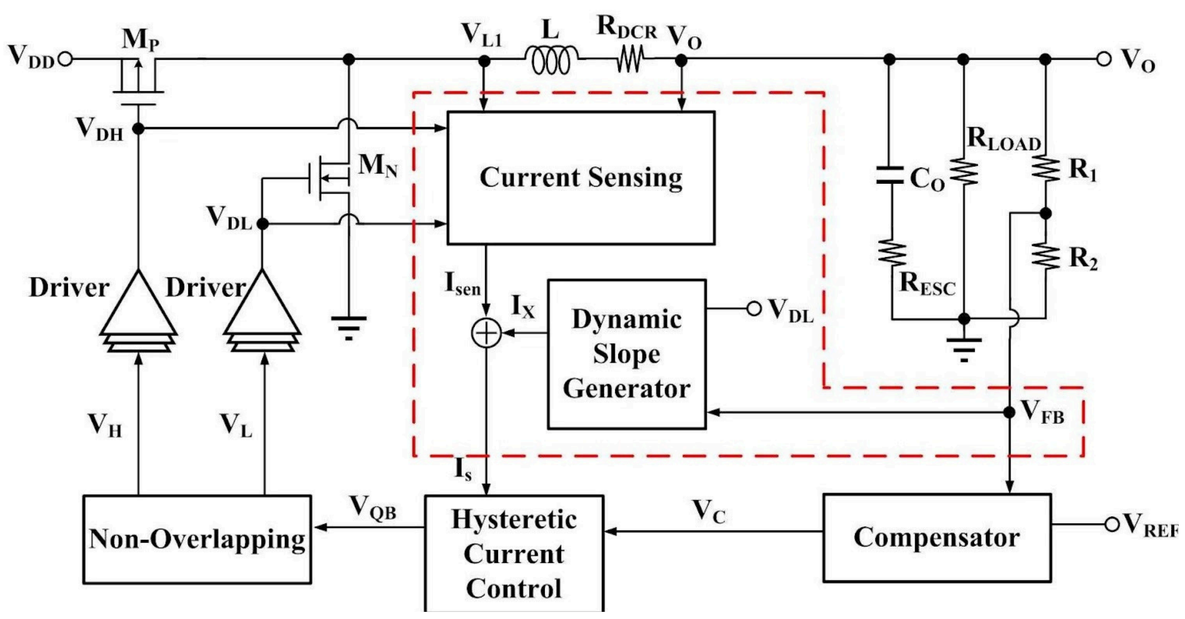
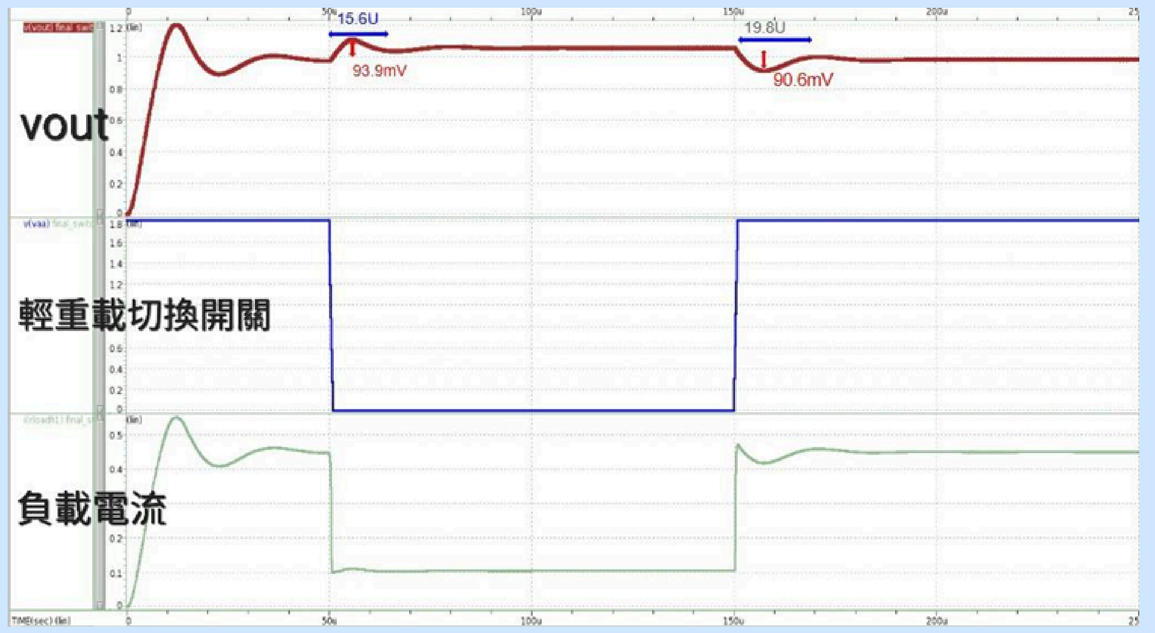
電路圖 Circuit



模擬圖 Simulation



摘要 Abstract

本研究旨在設計並實現一個高效率、低漣波的電流控制多迴路遲滯降壓轉換器架構。主要目標包括：穩定輸出電壓，在寬輸入電壓範圍，使輸出電壓穩定於約 1.1 V，以滿足低壓系統供電需求；降低輸出漣波，以提升電源品質；提高轉換效率，使最高效率可達 90%以上；提升負載突變下的暫態響應。

本設計採用UMC 0.18 um Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process製程實作，並透過模擬與測試驗證電流控制多迴路遲滯降壓轉換器架構在低壓、高效率降壓轉換器中的可行性。 此電路的設計目的是將輸入電壓 VDD 轉換成穩定的輸出電壓 Vo，並且能夠在不同的負載條件下仍能維持良好的穩壓特性。

運作原理 Principle

首先，輸出電壓經由一對電阻分壓後送入補償器（Compensator）與參考電壓進行比較，產生的控制電壓能夠設定電流控制器之工作基準。其次，電感電流則透過電流偵測電路（CurrentSensing）轉換為感測訊號，並經由動態斜率補償器（Dynamic Slope Generator）進行修正，以避免高頻操作下產生次諧波震盪。修正後的電流訊號與控制電壓於遲滯比較器（HystereticCurrent Control）中進行比較，決定功率電晶體的導通與關閉時機，從而使電感電流受限於預設之上下邊界，達到快速暫態響應與穩定輸出的效果。最終，經過非重疊電路（Non-Overlapping）與閘極驅動器（Driver），控制訊號被轉換為對功率電晶體的驅動，確保輸出電壓於負載突變時仍能快速回復並維持穩定。

綜合而言，本架構以電壓回授決定輸出目標，藉由電流回授即時調整開關，最後驅動 MOSFET 進行電感充放電，從而在負載變化下仍能維持輸出電壓的快速且穩定的控制。

實作成果 Outcome

全電路模擬	模擬結果		
轉換效率	94.57%(Iload=450mA)		
輸出電壓漣波	輸入電壓	輸出電壓漣波	
	1.6V	2.077mV	
	1.8V	2.0918mV	
	2.0V	2.1424mV	
負載調節率	2.32mV/A		
線性調節率	0.022%		
暫態響應	重載轉為輕載	Overshoot (mV)	93.9
		Settling Time (us)	15.6
	輕載轉為重載	Undershoot (mV)	90.6
		Settling Time (us)	19.8

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